

FIG. 1

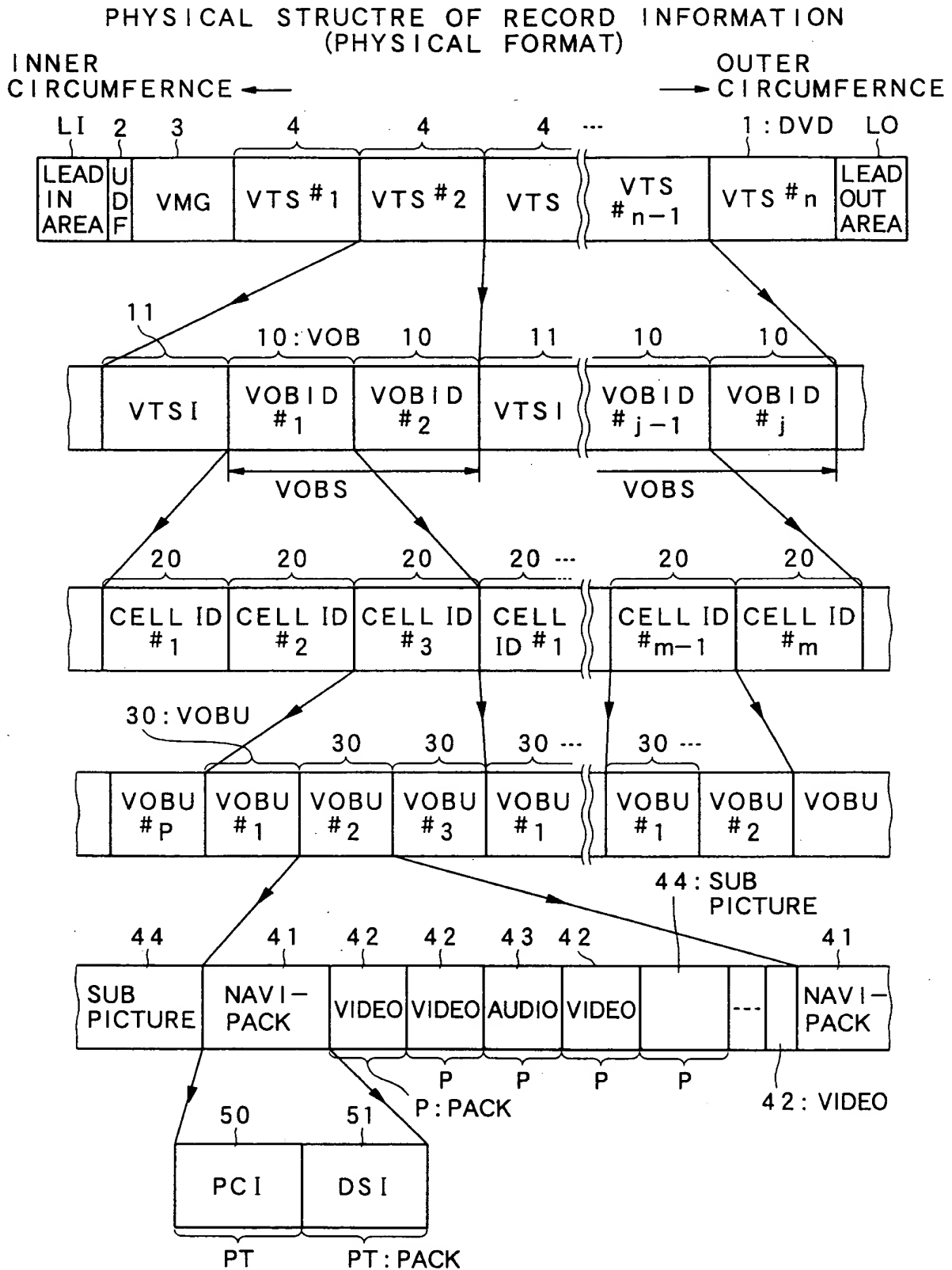


FIG.2

LOGICAL STRUCTURE OF RECORD INFORMATION (LOGICAL FORMAT)

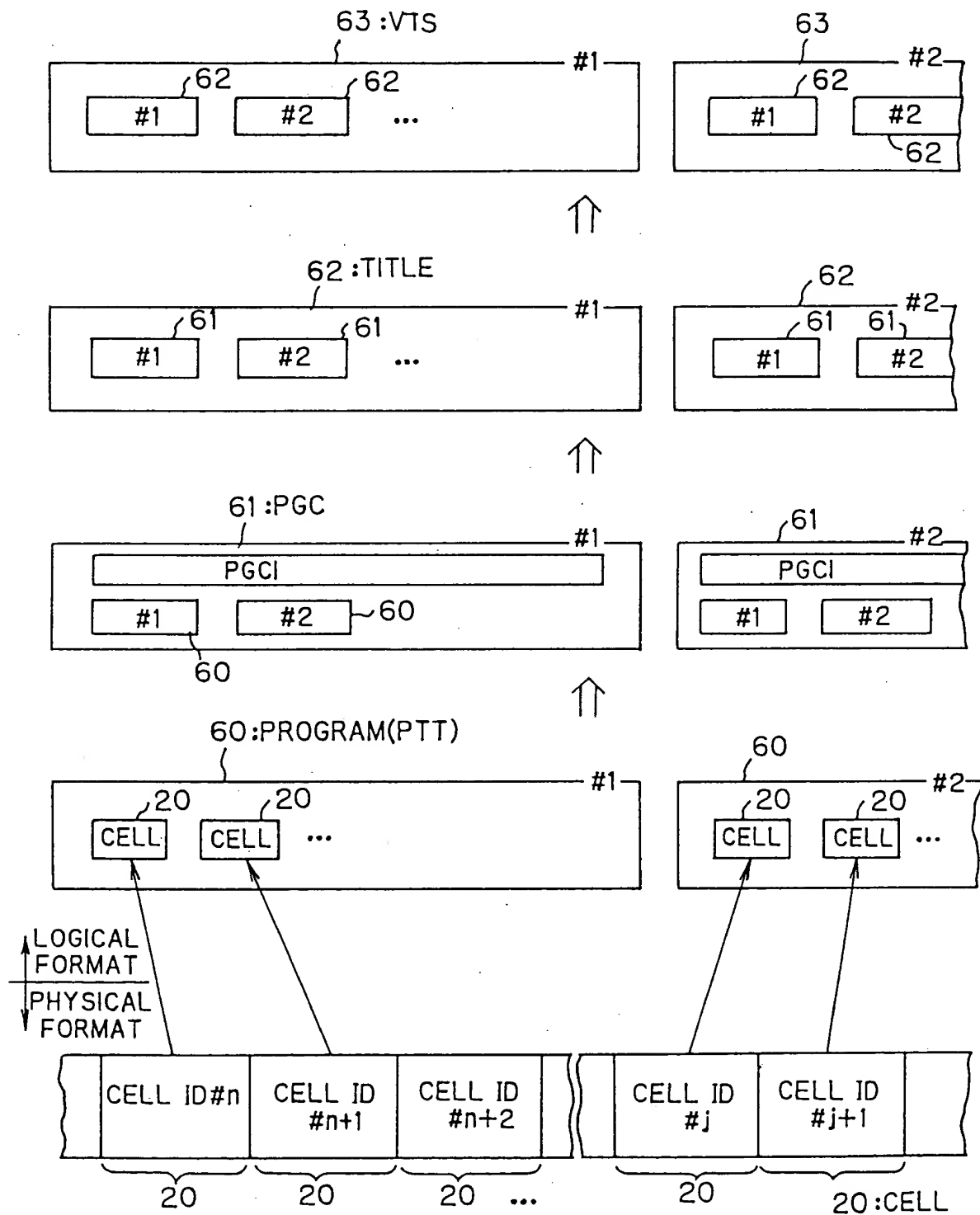


FIG. 3

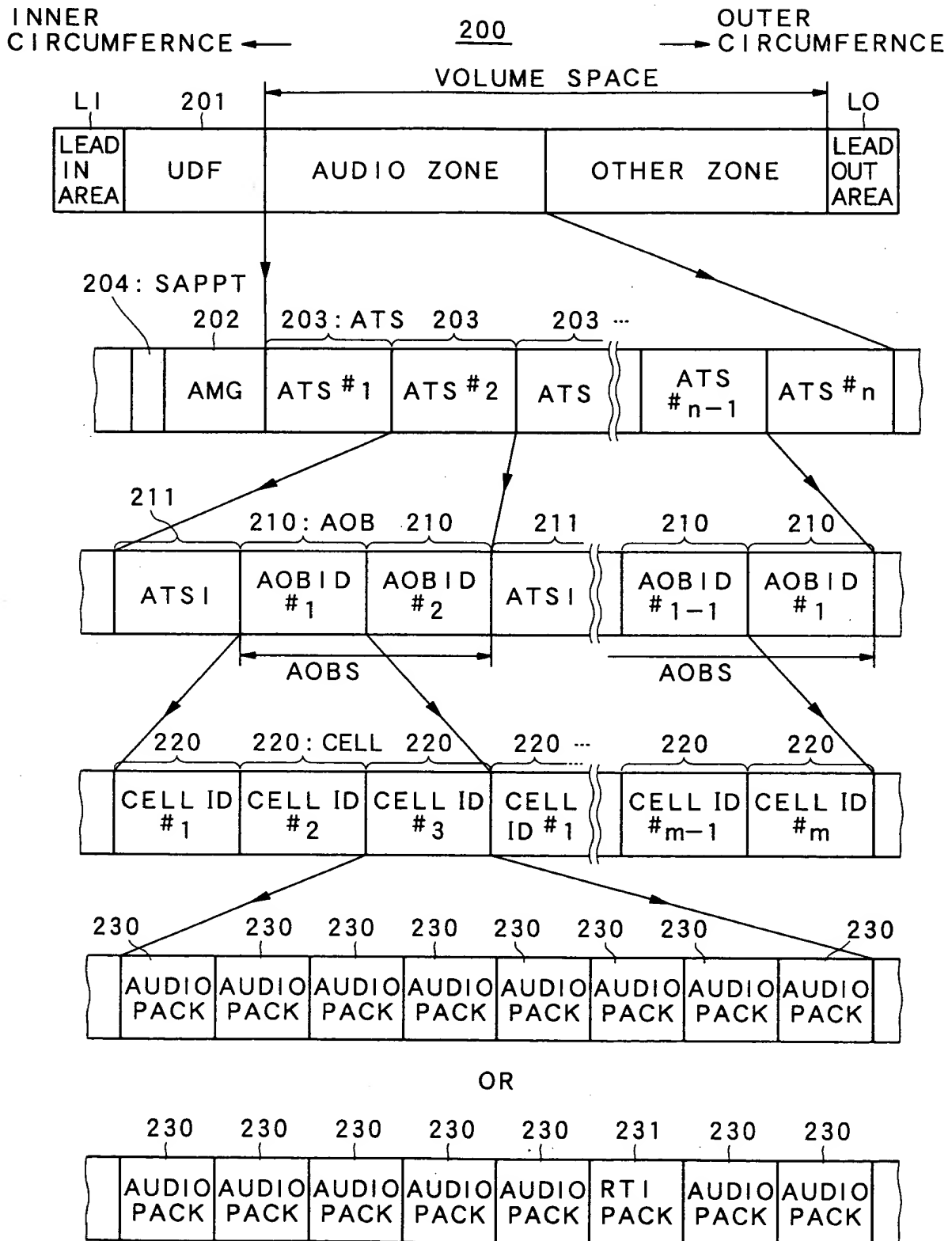
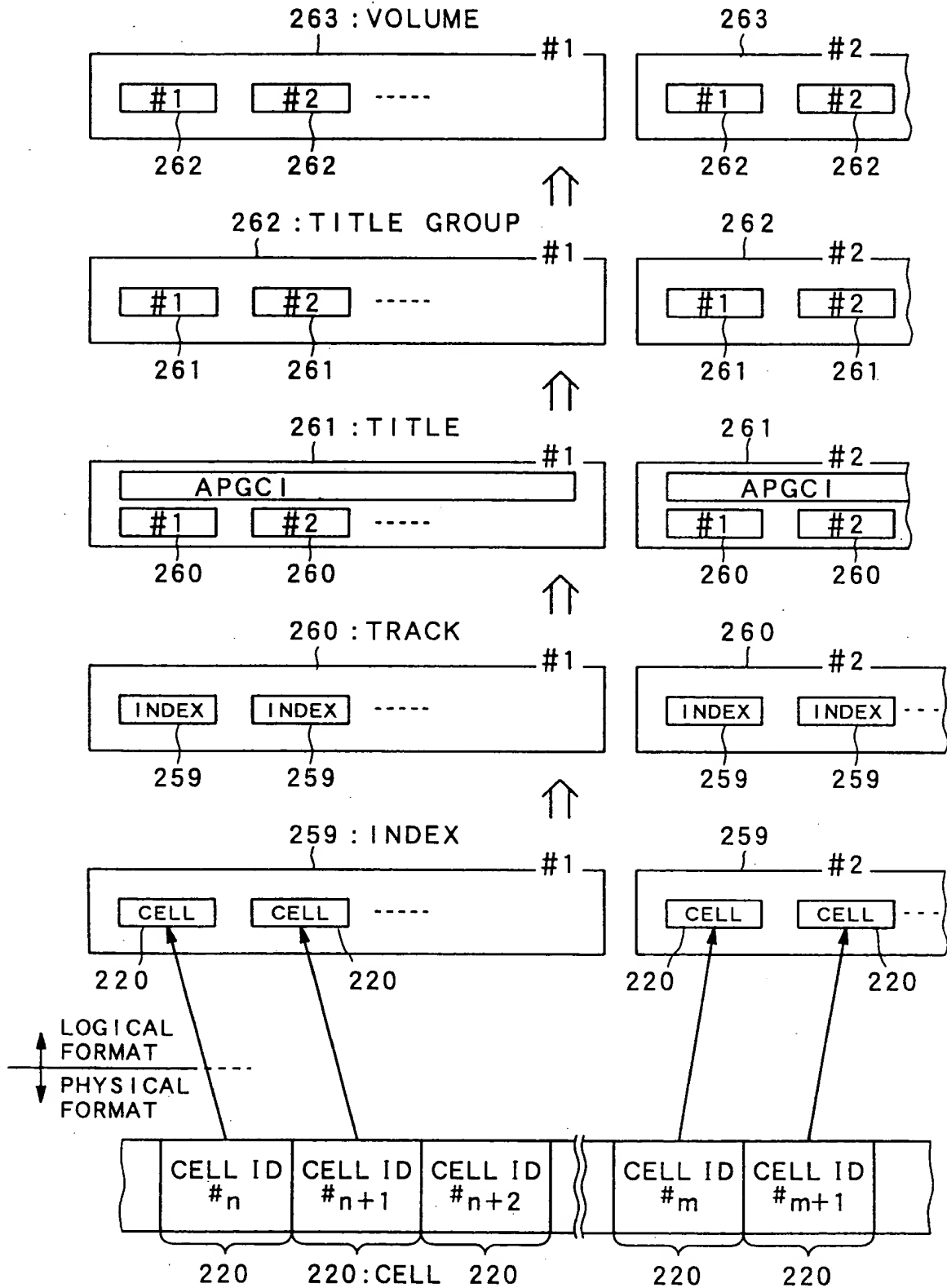
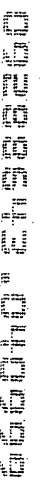
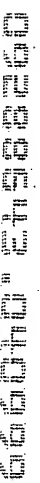


FIG. 4



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The diagram illustrates the structure of a video stream and its mapping to a PGC track. At the top, a PGC track labeled "PGC 1" is shown. Below it, the video stream is organized into two main sections: "VIDEO PROGRAM #2" and "VIDEO PROGRAM #3". "VIDEO PROGRAM #2" contains "VIDEO CELL #4". "VIDEO PROGRAM #3" contains "VIDEO CELL #6". These cells are mapped to a sequence of video cells: "VIDEO CELL #4", "VIDEO CELL #5", and "VIDEO CELL #6". Below the video cells, there are tracks for "AUDIO DATA", "FEATURE DATA", and "AUDIO DATA". The "AUDIO DATA" tracks are mapped to "AUDIO CELL #2" and "AUDIO CELL #3". At the bottom, the "AUDIO PROGRAM #1" and "AUDIO PROGRAM #2" are shown, with "AUDIO CELL #1" and "AUDIO CELL #2" respectively. The "AUDIO PROGRAM #1" is mapped to "AUDIO CELL #1" and "AUDIO CELL #2", and the "AUDIO PROGRAM #2" is mapped to "AUDIO CELL #3". The "PGC 1" track is mapped to the "AUDIO PROGRAM #1" and "AUDIO PROGRAM #2".

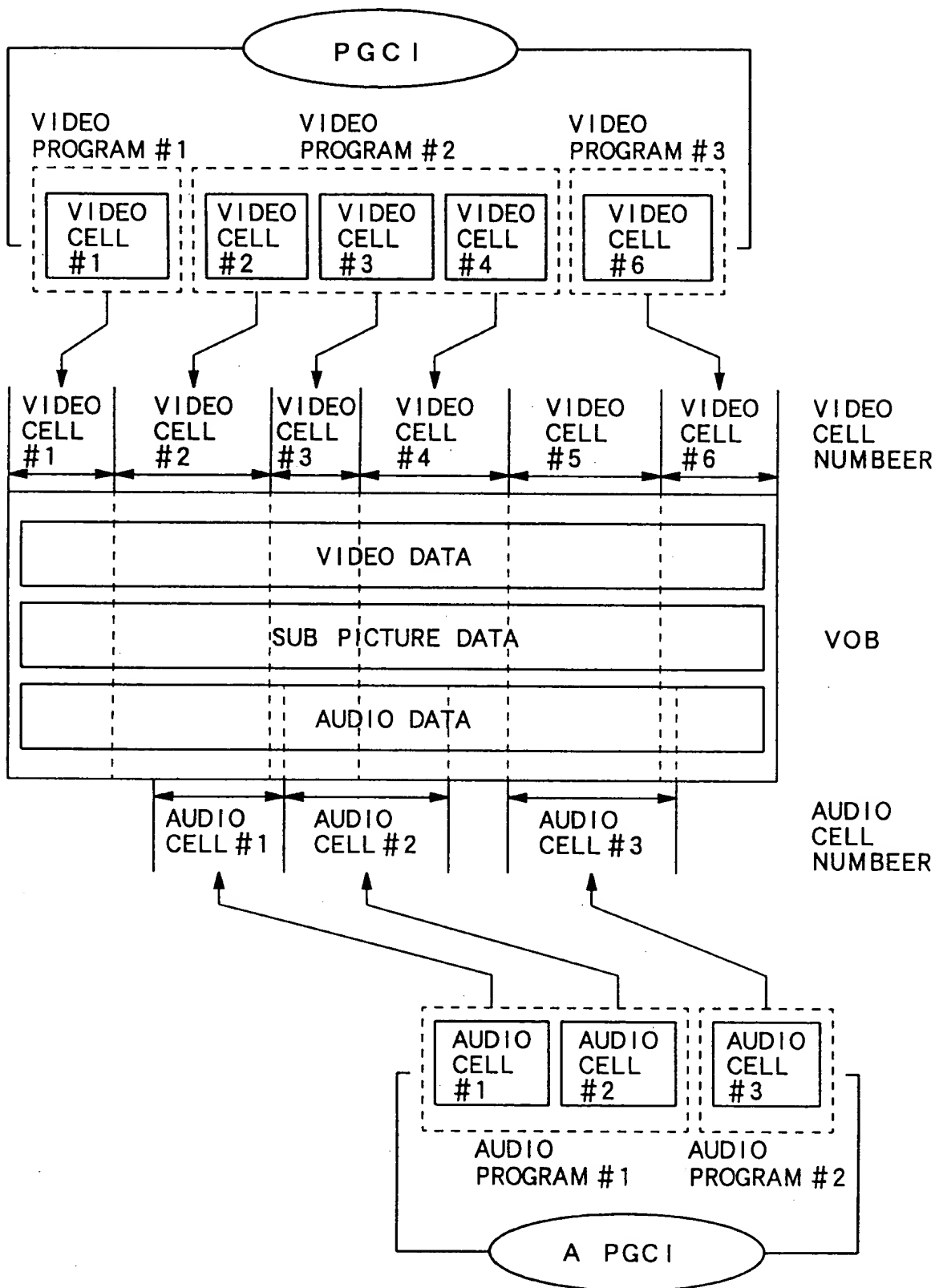
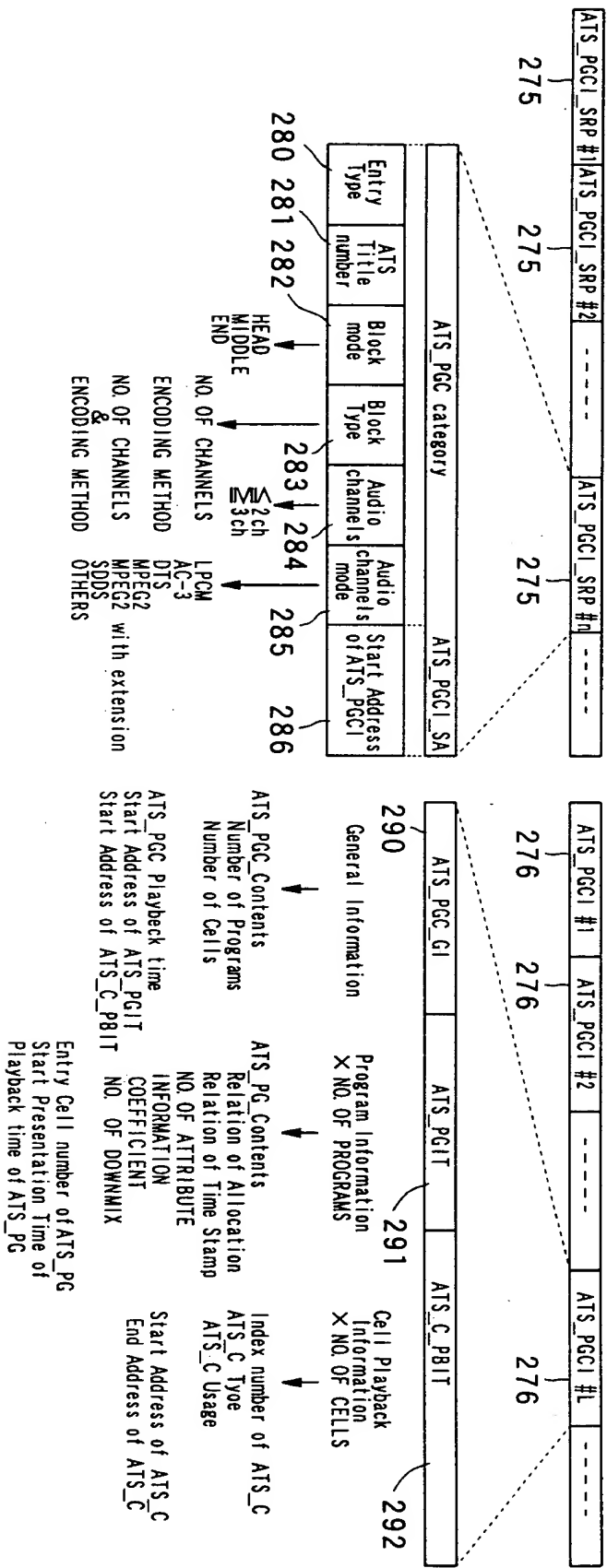


Figure 1 is a block diagram of a video recording system. The diagram is organized into three main sections: AUDIO ZONE, VIDEO ZONE, and LEAD IN AREA. The AUDIO ZONE includes blocks for audio signals (P1A, P1V, P1C, P3V, P4C) and audio processing blocks (ATSI, VMGI, TT_SRP, TT_SRP#1-5). The VIDEO ZONE includes blocks for video signals (P1A, P1V, P1C, P3V, P4C) and video processing blocks (VTSI, VOB, VTS#1, VTS#2, VMGI, TT_SRP, TT_SRP#1-5). The LEAD IN AREA includes blocks for lead in signals (P1A, P1V, P1C, P3V, P4C) and lead in processing blocks (VTSI, VOB, VTS#1, VTS#2, VMGI, TT_SRP, TT_SRP#1-5). The diagram shows the flow of data from input signals to output signals, with various processing blocks and signal paths.

[illegible]

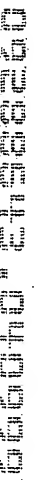
FIG. 9B



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The diagram illustrates a navigation information structure. At the top, a box labeled 'Title #1 (2ch/Multi)' (261) contains three 'Track' entries (260): 'Track #1', 'Track #2', and 'Track #3'. Below this, a large diamond shape represents 'USER'S RECOGNITION'. This diamond is connected to two main program blocks: 'PGC #1 (for 2ch)' (300) and 'PGC #2 (for Multi channel)' (300). Each PGC block contains a list of 'Program' entries (301) and 'Cell' entries (220). For PGC #1, the programs are 'Program #1', 'Program #2', and 'Program #3', each associated with a set of cells (e.g., 'Cell #1' through 'Cell #7'). For PGC #2, the programs are 'Program #1', 'Program #2', and 'Program #3', each associated with a set of cells (e.g., 'Cell #1' through 'Cell #7'). Arrows indicate the flow from the tracks through the user's recognition to the specific programs and cells. A 'PGC Block STRUCTURE' is shown as a grid of cells (210) for each PGC, with 'AOB #1 (for 2ch)' and 'AOB #2 (for Multi channel)' indicating specific areas of interest. A 'NAVIGATION INFORMATION' arrow points to the right, and a 'SUBSTANTIAL INFORMATION' arrow points to the left.

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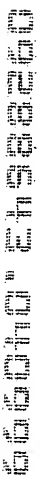
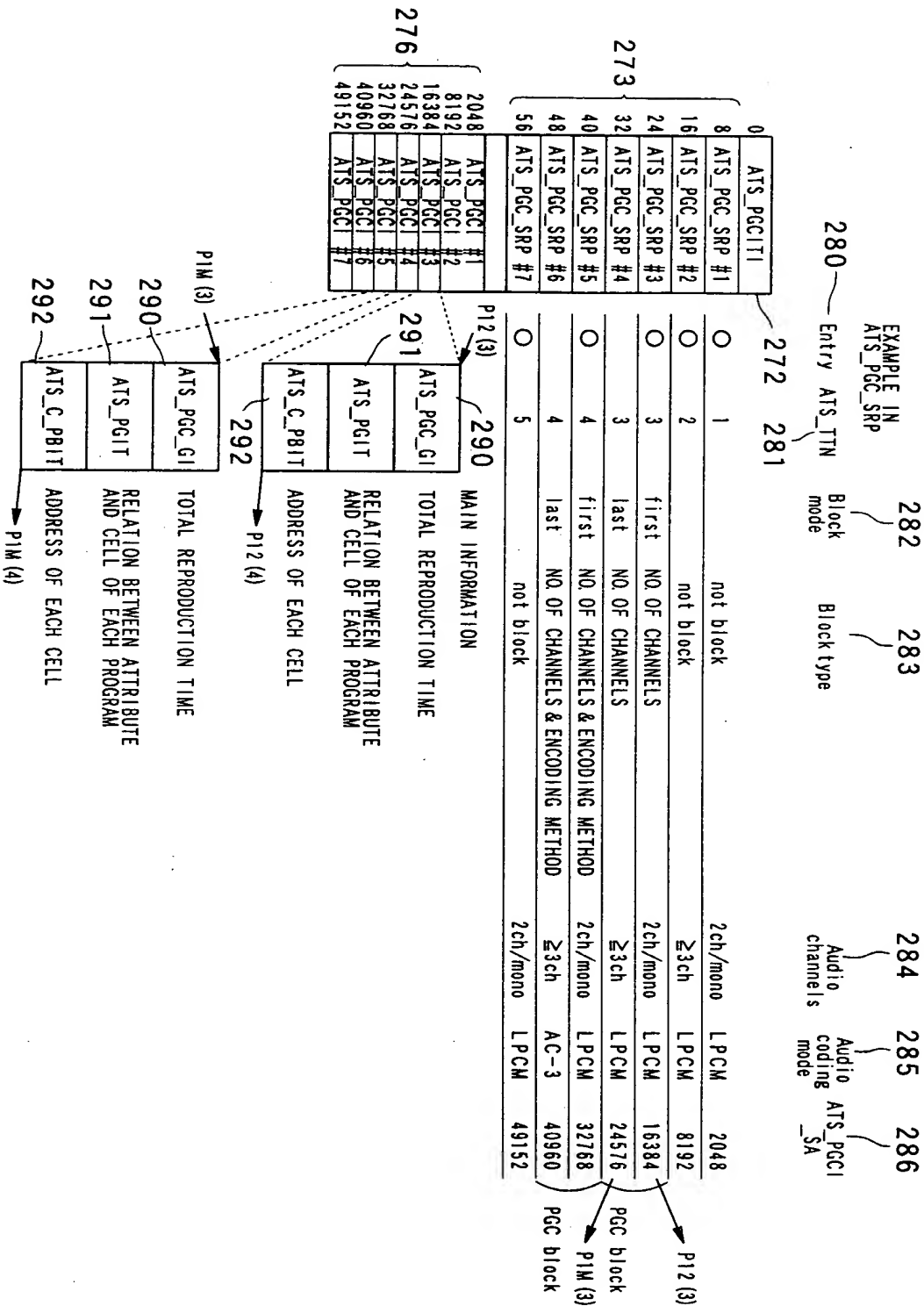


FIG. 12B



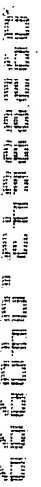


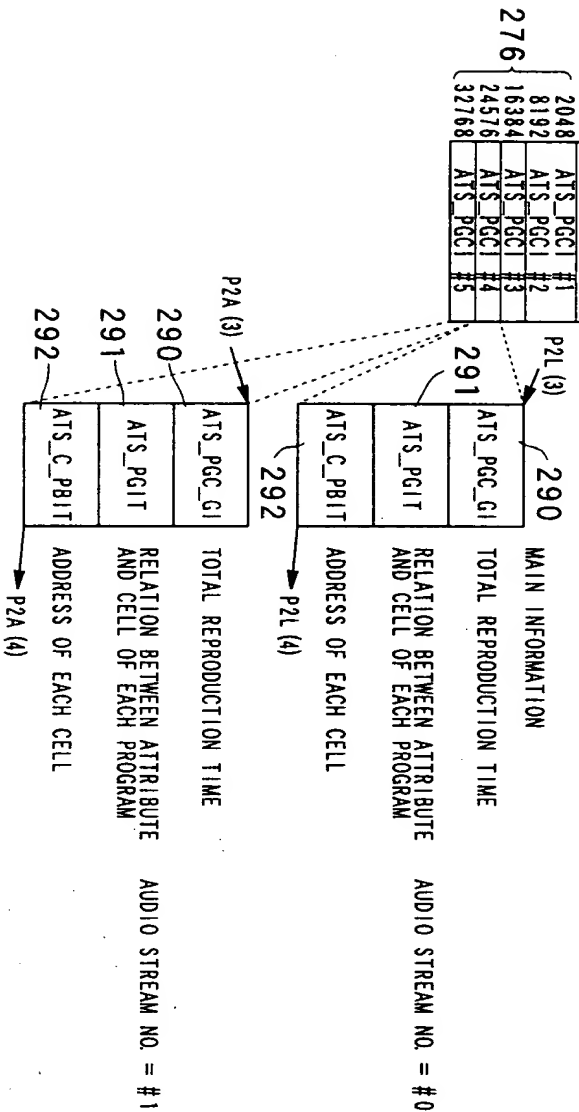
FIG.13B

EXAMPLE IN
ATS_PGC_SRP

Entry	ATS_TTN	Block mode	Block type	Audio channels	Audio coding mode	ATS_PGC1
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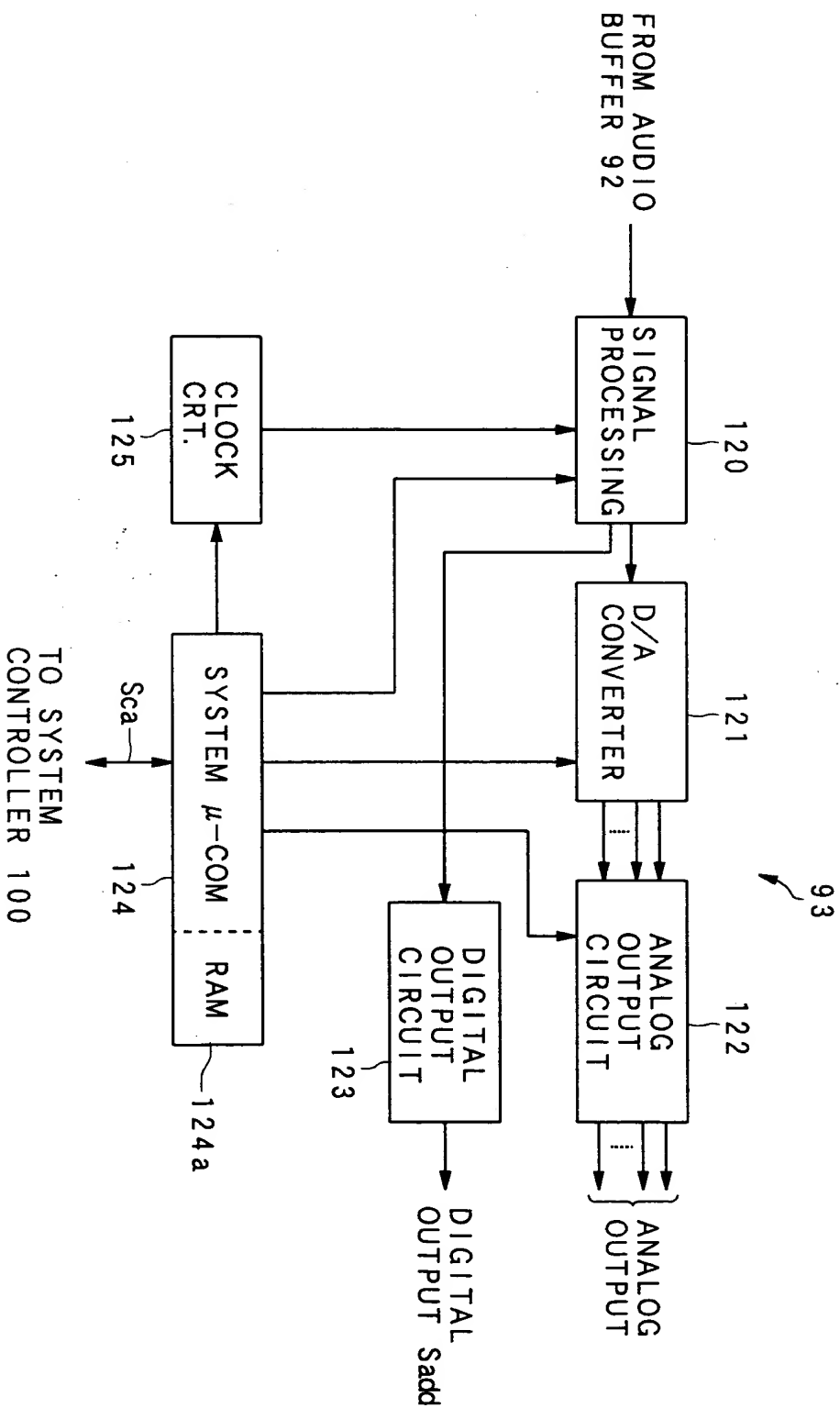
272						
0	ATS_PGCITI					
8	ATS_PGC_SRP #1	O	1	not block	2ch/mono	LPCM 2048
16	ATS_PGC_SRP #2	O	2	not block	2ch/mono	LPCM 8192
24	ATS_PGC_SRP #3	O	3	not block	2ch/mono	LPCM 16384
32	ATS_PGC_SRP #4	O	4	first NO. OF CHANNELS & ENCODING METHOD	2ch/mono	LPCM 24576
40	ATS_PGC_SRP #5		4	last NO. OF CHANNELS & ENCODING METHOD	≥3ch	AC-3 32768

PGC block
P2A (3)



The diagram illustrates the internal components and signal flow of a video cassette recorder. At the top, a tape (1) is shown with a read/write head (80) and a spindle (B). The SPINDLE MOTOR (102) and SLIDER MOTOR (103) are connected to a DRIVE CONTROLLER (101). The DRIVE CONTROLLER (101) is also connected to a DEMODULATE & CORRECT block (81). The DEMODULATE & CORRECT block (81) is connected to a TRACK BUFFER (83) and a SYSTEM BUFFER (85). The TRACK BUFFER (83) is connected to a DEMULTIPLEXER (86). The SYSTEM BUFFER (85) is connected to the DEMULTIPLEXER (86). The DEMULTIPLEXER (86) is connected to an AUDIO BUFFER (92) and an RTI BUFFER (95). The AUDIO BUFFER (92) is connected to an AUDIO DECODER (94). The RTI BUFFER (95) is connected to an RTI DECODER (96). The RTI DECODER (96) is connected to an RTI DECODER BUFFER (97). The AUDIO DECODER (94) is connected to an AUDIO DECODER BUFFER (94). The AUDIO DECODER BUFFER (94) is connected to an output (O). The SYSTEM CONTROLLER (100) is connected to the DRIVE CONTROLLER (101), DEMODULATE & CORRECT (81), TRACK BUFFER (83), SYSTEM BUFFER (85), DEMULTIPLEXER (86), AUDIO BUFFER (92), RTI BUFFER (95), AUDIO DECODER (94), and RTI DECODER (96). The SYSTEM CONTROLLER (100) is also connected to an INPUT UNIT (98) and a DISPLAY (99). The INPUT UNIT (98) is connected to the SYSTEM CONTROLLER (100). The DISPLAY (99) is connected to the SYSTEM CONTROLLER (100). The SYSTEM CONTROLLER (100) is connected to a HEADPHONE JACK (400). The HEADPHONE JACK (400) is connected to the SYSTEM CONTROLLER (100). The SYSTEM CONTROLLER (100) is connected to a MEMORY (100a). The MEMORY (100a) is connected to the SYSTEM CONTROLLER (100).

FIG. 16



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FIG.17A

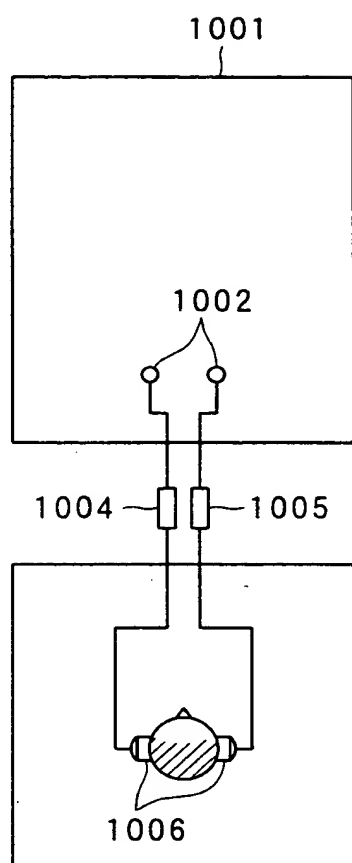
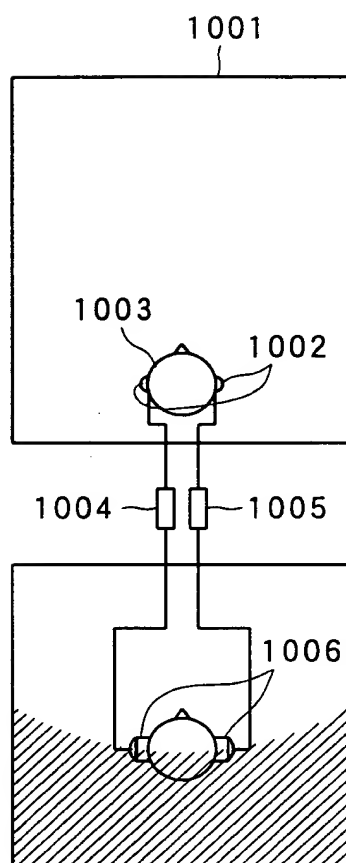


FIG.17B



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APPROVED	O.G. FIG.	
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FIG.18

AUDIO PACK 230							
#1	#2	#1	#2	#1	#2	#1	
STEREO	BINAURAL	STEREO	BINAURAL	STEREO	BINAURAL	STEREO	

FIG.19

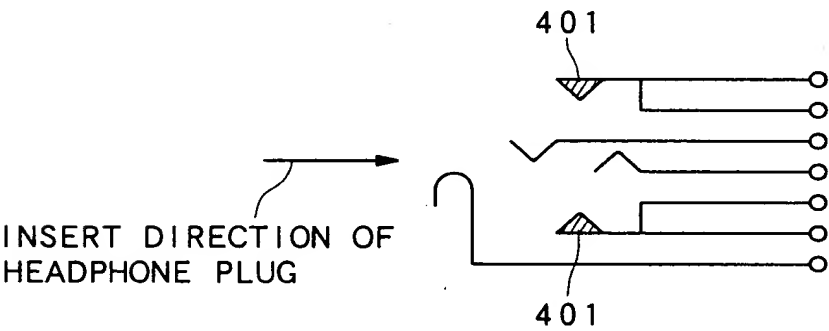


FIG. 20

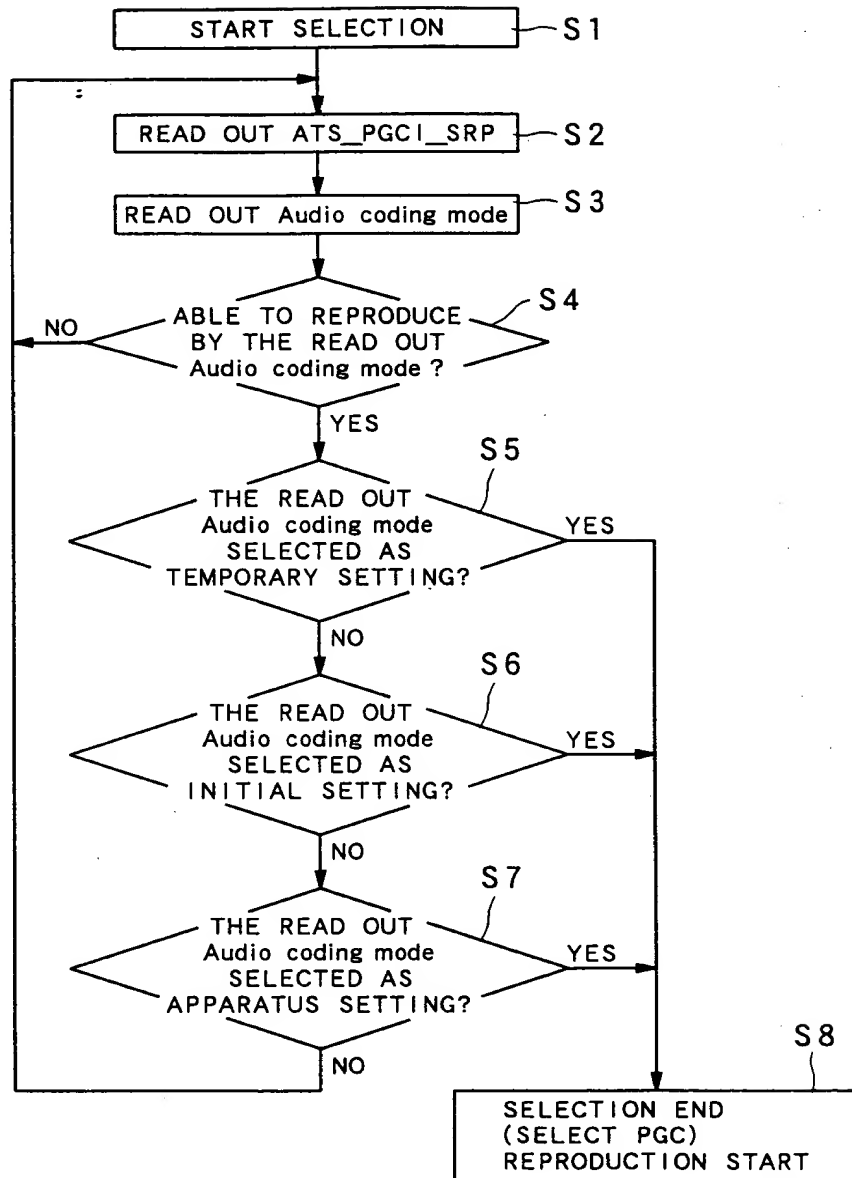
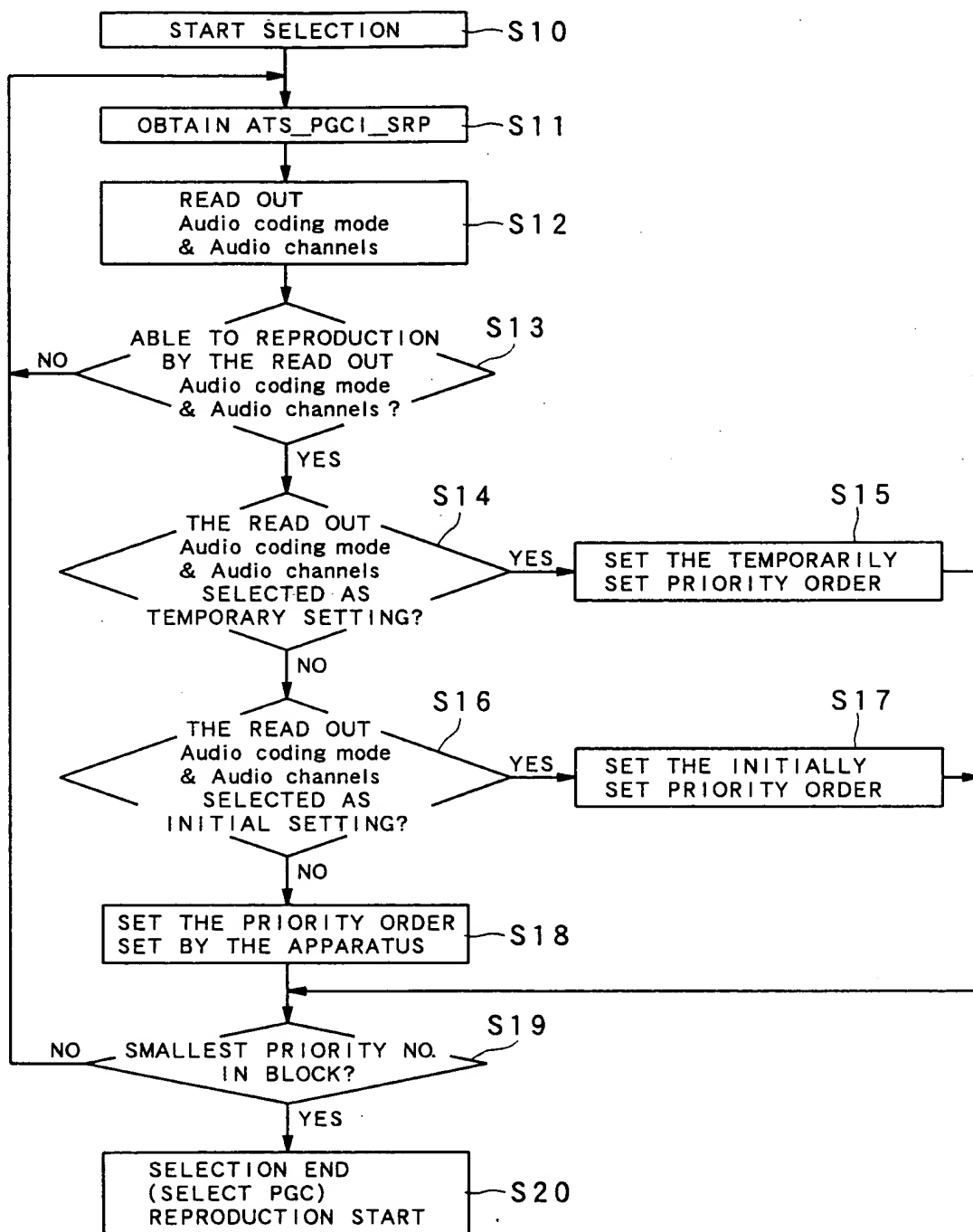


FIG. 21



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